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Design strategy and working principle of GaN vertical trench gate MOSFETs with p-type shielding rings

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Shielding ring (SR) structures are widely employed beneath the gate trench of vertical trench gate MOSFETs for the purpose of enhancing the gate oxide reliability and avoiding premature breakdown. To facilitate an in-depth understanding of the vertical power MOSFETs with p-type SRs (SR-MOSFETs), we numerically investigated the influence of the key parameters on the static characteristics of GaN-based vertical power SR-MOSFETs by TCAD simulation. We comprehensively elucidated the reach-through and non-reach through behaviors in the SR structures with different thicknesses, widths, and p-doping concentrations. We also illustrated the quasi-saturation effect by analyzing the 2D electron distribution and current density at the pinch-off point. With the same off-state voltage levels as conventional vertical MOSFETs, the SR-MOSFETs feature reduced on-state resistance and improved switching performance, which can provide theoretical guidance towards the development of high performance vertical gallium nitride power MOSFETs.

1. Introduction

Power transistors are widely applied in high-voltage power converters, fast charging systems, and electric vehicles.[1)] Traditional silicon (Si)-based power transistors have reached their theoretical limits due to the drawbacks of the material properties.[2)] Gallium nitride (GaN), characterized by its excellent properties of wide bandgap, large critical electric field and exceptional thermal stability, has drawn much attention as an appealing candidate material for power transistors.[3,4)]

Thanks to the two-dimensional electron gas (2DEG) generated at the AlGaN/GaN heterointerface,[5)] GaN-based lateral high electron mobility transistors (HEMTs) have been extensively commercialized for low and medium voltage applications. However, for high-power and kilovolt applications, considerable gate-to-drain spacing of the HEMTs is required, which leads to a limited operating frequency of the devices since the parasitic components and footprint of the HEMTs scale directly proportionally with the gate-to-drain spacing.[6)] Moreover, the 2DEG channel of the HEMTs locates near the device surface, making it extraordinarily susceptible to the surface states. Fortunately, vertical device topologies can avert these issues. A high breakdown GaN vertical device can be simply achieved by increasing the vertical thickness of the drift region, without increasing the device footprint and introducing additional parasitic components. Besides, current collapse issues can be also addressed by the GaN vertical topologies.

Given the unique benefits over their lateral counterparts, various GaN-based vertical transistors have been demonstrated, such as fin power FETs (FinFETs),[7)] current aperture vertical electron transistors (CAVETs),[8,9)] junction FETs (JFETs),[10)] and trench MOSFETs (T-MOSFETs).[11–14)] Amongst these vertical GaN power transistors, T-MOSFETs have been extensively explored due to their relatively simple fabrication process and positive threshold voltage exceeding 3 volts. Moreover, the T-MOSFETs also possess avalanche capability to insure against the surge voltage from the stray inductance of the circuit during switching.[15)] However, due to the locally plethoric electrostatic interaction effect under blocking conditions, a crowded electric field is typically generated at the corners of the gate trench, which leads to degraded gate dielectric reliability and premature breakdown of the T-MOSFETs. Therefore, it is of great significance to modulate the crowded electric field at the proximity of the gate trench for the purpose of enhancing the blocking capability and improving the gate stack reliability of vertical power MOSFETs.

A shielding ring (SR) structure beneath the gate trench has been reported in SiC-based MOSFETs to address the issue. Tan et al.[16)] proposed and fabricated the first trench MOSFETs with SR structures by self-aligned p-type implantation. Subsequently, the SR structure was widely adopted in experimentally fabricated SiC MOSFETs for high voltage applications.[17–22)] To elucidate the working principles of the SR structure, several numerical studies have been reported, covering both the dynamic and static characteristics. Wei et al.[23,24)] simulated the dynamic performance of SiC MOSFETs with SR structures and demonstrated the effectiveness of this structure to improve the switching speed of SiC MOSFETs. Kyoung et al.[25)] studied the influence of the p-SR thickness and trench depth on the on-state performance of SiC MOSFETs. The impact of the p-doping concentration in the SR structure on the value of the electric field in the gate oxide was also investigated, under the condition of a fixed thickness and width of the p-SR structure.

Although the electric field distribution is one of the determining factors for the breakdown behavior, it would be more convincing and straightforward to present the breakdown voltage of the devices with different design parameters. Moreover, during the actual fabrication process, the thickness and width of the p-SR structure may vary, which can result in a distinct impact of the p-doping concentration on the electric field distribution at off-state. Therefore, it is highly demanded to conduct a comprehensive parametric investigation of the p-SR structure by taking all the key design parameters into consideration and fulfil a complete design strategy for high performance trench gate MOSFETs with p-SR structures (SR-MOSFETs). So far, there has been no systematic investigation on the SR-MOSFETs, regardless of Si, SiC or GaN materials. In addition, the working principles of the SR-MOSFETs

remains to be explored, e.g. the reach-through behavior in the shielding rings of the SR-MOSEFTs and the quasi-saturation effect occurred in the output characteristics. Furthermore, considering the unique material properties of GaN, the study on SiC MOSFETs cannot be directly used to guide the experimental development of vertical GaN MOSFETs.

In this paper, we systematically investigate the influence of the key structural parameters on the off-state and on-state characteristics of the SR-MOSFETs, by varying the doping concentration, thickness, and width of the p-SR structure. The breakdown voltages of the devices are extracted to quantitatively compare the off-state characteristics of the SR-MOSFETs with different design parameters, by including the Selberherr impact ionization model with carefully calibrated simulation coefficients. The field-dependent mobility model and spice model are also considered for the on-state and dynamic performance of the devices. Moreover, we comprehensively explore and elucidate the reach-through and non-reach through behaviors in the SR structures with different thicknesses, widths, and p-doping concentrations. We also illustrate the quasi-saturation effect in the SR-MOSFETs by analyzing the 2D electron distribution and current density at pinch-off point. The on-resistance model has also been re-derived considering the unique structure of the proposed SR-MOSFETs. We believe that the results can lead to a complete design strategy and an in-depth understanding of the SR-MOSFETs.

This paper is organized as follows. Sect. 2 shows the device architectures and the blocking working mechanism of the SR-MOSFETs. In Sect. 3, we investigate the effect of the key structural parameters [e.g. the p-doping concentration ($N_{p\text{-}SR}$), thickness (T), and width (W)] of the p-SR on the blocking performance by analyzing the electric field distribution. Furthermore, we re-derive an on-resistance model and elucidate the QS effect of SR-MOSFETs. Dynamic performance is also observed for the SR-MOSFETs with identical voltage levels as conventional MOSFETs. Finally, in Sect. 4, this paper is concluded.

2. Device architectures and principles

Figures 1(a)–1(c) illustrate the schematic cross sections as well as the electric field distribution of the conventional GaN T-MOSFETs and the proposed GaN SR-MOSFETs. Both devices feature a trench gate structure, except that a p-SR is incorporated beneath the gate trench of the SR-MOSFETs. In order to illustrate the working principle of the SR-MOSFETs, one-dimensional (1D) electric field distributions are extracted for the T-MOSFETs and SR-MOSFETs along the sidewalls of the gate trench at the identical bias voltage, as shown in Fig. 1(b). It can be observed that the T-MOSFETs exhibit a triangular electric field distribution and the peak electric field occurs at the trench corners which results in the premature breakdown of the devices. By incorporating p-SRs beneath the gate trench, part of the electric field at the trench corners can be transferred to the edges of embedded p-SRs, resulting in a more uniform double-peak distribution of the electric field at the vicinity of the gate trench corners and a p–n$^-$ junction region. Compared with the T-MOSFETs, the peak electric field can be efficiently moderated for the SR-MOSFETs at identical bias voltage, preventing premature breakdown at the trench corners.

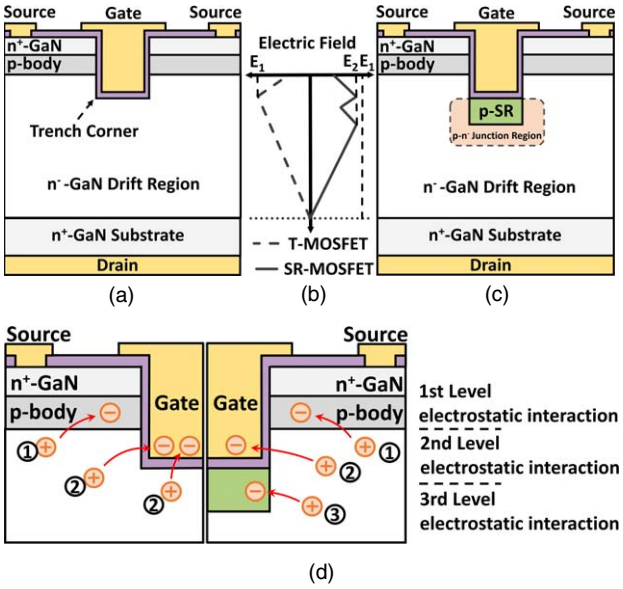

Fig. 1. The cross-sectional views of the (a) T-MOSFETs and (c) SR-MOSFETs. (b) The electric field distribution in the T-MOSFETs and SR-MOSFETs at the same bias voltage. (d) The working mechanisms of tri-level electrostatic interactions in the T-MOSFETs and SR-MOSFETs.

To explain the mechanism behind the electric field regulation by the embedded p-SRs, Fig. 1(d) illustrates the tri-level electrostatic interactions at the proximity of the gate trench. For both the conventional T-MOSFETs and SR-MOSFETs, two levels of self-assembled electrostatic interactions are induced intrinsically from the p-body and trench gates, respectively. By incorporating a p–n$^-$ junction region formed by the p-SR structure beneath the gate trench, a third-level electrostatic interaction can be introduced in the SR-MOSFETs, effectively moderating the excessive electrostatic interaction at the gate trench and allowing for significant improvement in the blocking capability.

In the following content, Technology Computer Aided Design (TCAD) simulations are carried out using the Advanced Physical Models of Semiconductor Devices (APSYS) software. The fundamental physical models used in the simulation include the impact ionization model, the field-dependent mobility model, and the spice model. The parameters are calibrated by fitting the breakdown voltage and on-state output current of the simulated devices to the experimental results from Ref. 11 as shown in Fig. 2.

The impact ionization coefficients for GaN are as follows:[26]

$$\alpha_n = 2.9 \times 10^8\ \mathrm{cm}^{-1} \times e^{\frac{-3.4\times10^7\ \mathrm{V\,cm}^{-1}}{E}} \quad (1)$$

$$\alpha_p = 1.34 \times 10^8\ \mathrm{cm}^{-1} \times e^{\frac{-2.03\times10^7\ \mathrm{V\,cm}^{-1}}{E}} \quad (2)$$

where E is defined as the magnitude of the electric field in the drift layer of the trench MOSFETs at the off-state.

3. Results and discussion

3.1. Effect of the doping concentration in the p-SRs on the electrical properties of the SR-MOSFETs

The effect of the p-doping concentration on the blocking characteristics of the SR-MOSFETs is investigated under different background doping concentrations in the drift

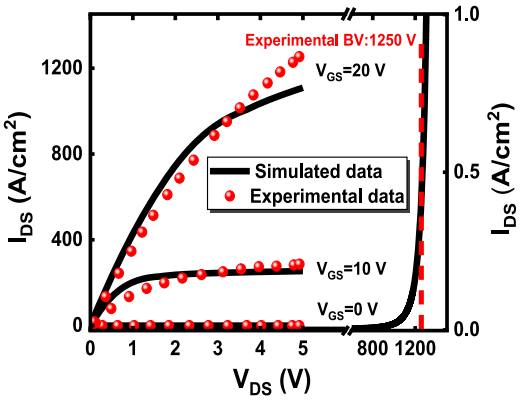

Fig. 2. Simulated and experimental on-state output current and the breakdown voltage of the T-MOSFETs.

region, as shown in Fig. 3(a). The p-doping concentration refers to the ionizable acceptor concentration and the breakdown voltage is extracted when the leakage current density reaches 0.1 A cm^{-2}. With increased p-doping concentration, the breakdown voltage of the SR-MOSFETs tends to initially increase and subsequently decrease. Notably, a peak breakdown voltage of 1467 V is recorded at the p-doping concentration of 9×10^{17} cm^{-3} for the SR-MOSFETs with a background doping concentration of 1×10^{16} cm^{-3} in the drift region, which is 29% higher than that of the T-MOSFETs (dotted line). Noteworthy, the breakdown voltage of the SR-MOSFETs is inversely correlated to the background doping concentration, owing to the reduced depletion width in the drift region at off-state. The peak breakdown voltages of 1746 V, 1467 V, and 872 V are obtained for the SR-MOSFETs with different doping concentrations of 7×10^{15} cm^{-3}, 1×10^{16} cm^{-3}, and 2×10^{16} cm^{-3} in the drift layer, respectively.

Figure 3(b) depicts the vertical electric field profiles of the T-MOSFETs and SR-MOSFETs along the oxide/GaN interface (dotted line in the inset) at a V_{DS} of 1000 V. The T-MOSFETs are characterized by a single electric field peak at the trench corners, which can induce premature breakdown of the devices. With embedded p-SRs beneath the gate trench (Devices A1–A3), part of the electric field at the trench corners of the T-MOSFETs can be transferred from the trench corners to the vicinity of the embedded p-SR edges and a double electric field peak can be observed in the electric field profiles of the SR-MOSFETs. Devices A1–A3 are chosen with the same p-SR thickness (0.2 μm) but different p-doping concentrations (3×10^{17} cm^{-3}, 9×10^{17} cm^{-3}, and 6×10^{18} cm^{-3}, respectively), as labeled in Fig. 3. An inappreciable fraction of the electric field is coupled to the p–n$^-$ junction region beneath the gate trench with a low p-doping concentration of 3×10^{17} cm^{-3}. Consequently, the premature breakdown still occurs at the trench corners and Device A1 exhibits a slightly increased breakdown voltage compared with the T-MOSFETs. As the p-doping concentration increases to 9×10^{17} cm^{-3} in Device A2, a relatively uniform electric field distribution can be obtained, which can result in the maximum breakdown voltage under a background doping concentration of 1×10^{16} cm^{-3}. However, when the p-doping concentration of p-SR further increases to 6×10^{18} cm^{-3} (Device A3), the electric field at the edges of p-SR exceeds the critical electric field of GaN, inducing a premature breakdown of the device.

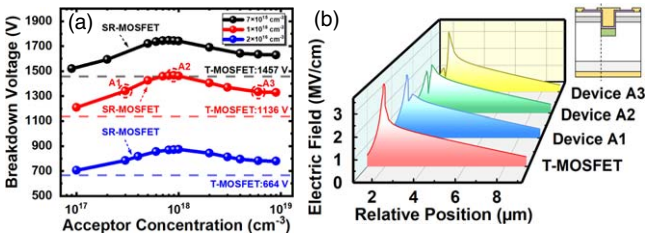

Fig. 3. (a) Breakdown voltage as a function of the acceptor concentration at a drift Conc of 7×10^{15} cm^{-3} (black solid line), 1×10^{16} cm^{-3}(red solid line), and 2×10^{16} cm^{-3} (blue solid line). The three dash lines correspond to the breakdown voltage of the T-MOSFETs at different background concentrations in the drift layer. (b) Electric field profiles along the oxide/GaN interface for the T-MOSFET, Device A1, A2 and A3.

3.2. Effect of the p-SR thickness on the electrical properties of the SR-MOSFETs

Aside from the p-doping concentration in the p-SR region, the thickness of p-SRs also plays a vital role in the redistribution of the electric field. Figure 4(a) illustrates the relationship between the breakdown voltage and the thickness of p-SRs for SR-MOSFETs at off-state. Regardless of the p-doping concentration of p-SRs, the breakdown voltage of SR-MOSFETs first increases and thereafter decreases with increased thickness of the p-SRs from 0 μm to 1 μm. Notably, a peak breakdown voltage of 1467 V is recorded at a thickness of 0.2 μm for the SR-MOSFETs with a p-doping concentration of 9×10^{17} cm^{-3} (Device A2). Moreover, despite of the similar peak breakdown values for the SR-MOSFETs with different p-doping concentrations, the optimal thickness to obtain the maximum breakdown voltage varies, which is reversely correlated with the p-doping concentrations.

To indicate the mechanism behind the phenomena above, we compare the two-dimensional (2D) electric field distribution of the SR-MOSFETs with different thicknesses of p-SRs at a V_{DS} of 800 V in Figs. 4(b)–4(e). Devices B1–B4 are chosen with identical p-doping concentration (5×10^{17} cm^{-3}) but different thicknesses of p-SRs (0.05 μm, 0.2 μm, 0.3 μm, and 0.6 μm, respectively), as labeled in Fig. 4(a). The 1D vertical electric field profiles of devices B1–B4 are extracted along the oxide/GaN interface. With increased p-SR thickness from 0.05 μm (device B1) to 0.6 μm (device B4), the electric field peak at the trench corners is gradually transferred to the vicinity of the p-SR edges. The

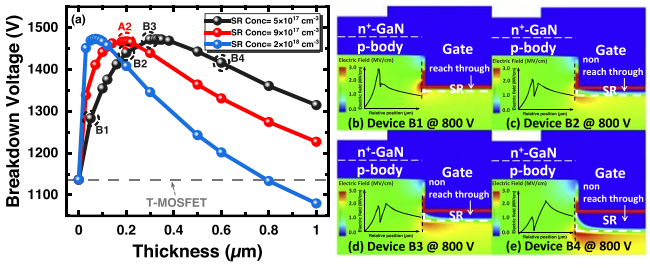

Fig. 4. (a) Breakdown voltage as a function of the thickness with the p-doping concentration of 5×10^{17} cm^{-3} (solid black line), 9×10^{17} cm^{-3} (solid red line), and 2×10^{18} cm^{-3} (solid blue line). The dash line corresponds to the breakdown voltage of the T-MOSFET. 2D electric field distribution in (b) Device B1, (c) Device B2, (d) Device B3, and (e) Device B4 at a V_{DS} of 800 V. 1D vertical electric field profiles of devices B1–B4 along the oxide/GaN interface (dotted line in the inset).

most uniform electric field distribution can be actualized with a p-SR thickness of 0.3 μm in device B3, leading to a significantly enhanced blocking capability. For devices B1, B2, and B4, a too thin or too thick p-SR will result in premature breakdown at either the gate trench corners or the p-SR edges due to the electric field crowding effect. Furthermore, it is worth noting that a reach-through (RT) behavior can be observed in device B1, in which the p-SRs are fully depleted beneath the gate trenches. For devices B2 to B4, the designed thicknesses of p-SRs are larger than the depletion width. Therefore, a non-reach-through (NRT) condition can be achieved with zero electric field recorded at the bottom of the trench, which effectively protects the gate dielectrics from the excess electric field and premature breakdown under stress conditions.

To further illustrate the RT behaviors of SR-MOSFETs at off-state, we intercept the vertical electric field profiles along the middle of the trench (dotted line in the inset) for the T-MOSFETs and SR-MOSFETs (Devices B1–B3 and A2) at a V_{DS} of 1000 V, as shown in Fig. 5. Due to the intrinsic electrostatic interaction at the trench gate structure, the excessive electric field can be observed in the gate dielectric layer of the T-MOSFETs. With increased p-SR thickness and p-doping concentration in the SR-MOSFETs, a dramatic reduction in the bottom oxide electric field (E_{ox}) can be observed, potentially leading to improved gate stack reliability. For the purpose of exploring the mechanism behind the decreased E_{ox}, we then look into the electric field distribution at the dielectric/p-SR interface, as shown in the inset of Fig. 5. Similar to the T-MOSFETs, the SR-MOSFETs with a p-SR thickness of 0.05 μm (device B1) feature a non-zero electric field value at the dielectric/p-SR interface (RT condition). Under this occasion, the p-SR is fully depleted and the ionized acceptors entirely participate in the coupling with the positive charges from the drift region. However, owing to the insufficient p-SR thickness, the electrostatic interaction between the gate electrode and the ionized donors in the drift region still persists at the bottom of the trench, resulting in an excessive electric field in the gate dielectric layer. With increased p-SR thickness to 0.2 μm in device B2, the value of the electric field at the interface drops to zero and the NRT condition occurs. The intrinsic electrostatic interaction at the bottom of the gate trench is fully screened and thus a dramatic reduction of the E_{ox} can be observed in Device B2. Moreover, an enlarged zero-electric field width can be observed with further increased p-SR thickness (Device B2 to B3) or p-doping concentration (Device B2 to A2), indicating a sufficient screening effect by the p-SR. Meanwhile, the excessive electric field at the gate dielectric layer is transferred to the bottom of the p-SR due to the enhanced electrostatic interaction between the p-SR and the drift region, leading to a further decrease in E_{ox}.

3.3. Effect of the p-SR width on the electrical properties of the SR-MOSFETs

After addressing the influences of the p-SR thickness on the blocking capability and the RT/NRT behaviors in the SR-MOSFETs, two groups of SR-MOSFETs are designed to illustrate the effects of the p-SR width and location on the electric field distribution and blocking characteristics of the devices, as shown as in Figs. 6(a) and 6(b). The p-SRs in group A extend from the middle of the trench to the trench corners while the p-SRs in group B fill the region from the trench corners to the middle of the trench. The lateral width of the p-SRs in groups A and B is 0 μm, 0.4 μm, 0.8 μm, 1.2 μm, 1.6 μm, and 2.0 μm, respectively. A minor increase in the breakdown voltage can be observed as the p-SR width increases from 0 μm (device C1) to 0.4 μm (device C2), and the breakdown voltage gradually increases from 1164 V to 1286 V as the p-SR further extends from 0.4 μm (device C2) to 1.6 μm (device C3) in group A, before a dramatic increase to 1467 V occurs when the p-SR extends to the trench corners (device A2). In Fig. 6(b), the breakdown voltage significantly increases as the p-SR width increases from 0 μm (device C1) to 0.4 μm (device C5) and then slightly increases as the p-SRs fill the region from 0.4 μm (device C5) to 2 μm (device A2), from which it can be concluded that the p-SR at the vicinity of the trench corners play a more crucial role in the breakdown characteristics than those close to the middle of the trench.

To explain the principle behind these phenomena, we intercept the electric field profiles from the SR-MOSFETs with different p-SR widths. Figures 7(a) and 7(b) show the lateral electric field distribution along the trench/p-SR interface (dotted line in the inset for the devices in group A (devices C2, C3 and A2) and group B (devices C1, C5 and

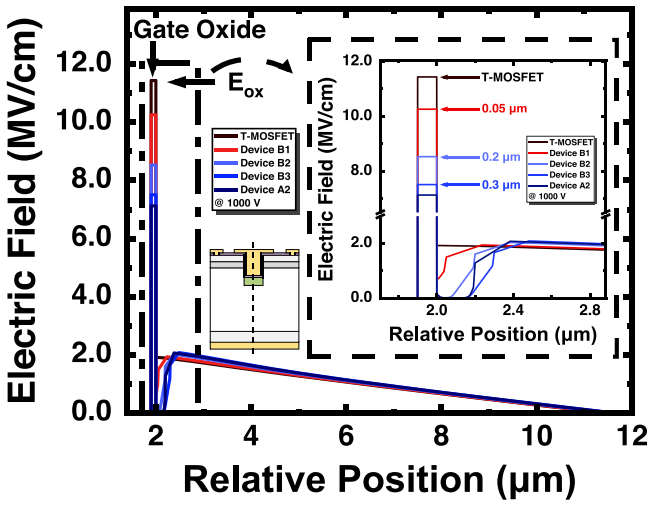

Fig. 5. Vertical electric field profiles along the middle of the trench at a V_{DS} of 1000 V. The inset shows the electric field distribution at the dielectric/p-SR interface.

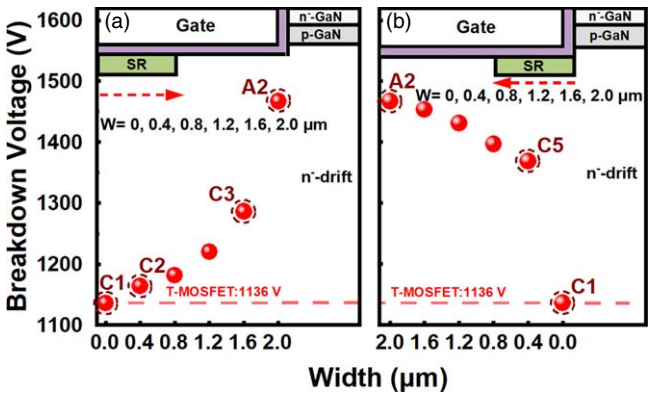

Fig. 6. (a) and (b) breakdown voltage as a function of the p-SR width in the SR-MOSFETs at the optimized design (T = 0.2 μm, p-doping concentration = 9×10^{17} cm^{-3}).

A2) at a V_{DS} of 1000 V, respectively. In Fig. 7(a), the peak value of the electric field at the trench corner in device C3 is slightly smaller than that in device C2 while the peak value of the electric field obviously decreases as the p-SR width increases to 2 μm (device A2), indicating the embedded p-SRs at the vicinity of the trench corners can significantly decrease the electric field peak at the trench corners of the SR-MOSFETs. Moreover, a near-zero electric field zone can be observed at the dielectric/p-SR interface with identical width to the p-SRs, which agrees with the aforementioned NRT condition discussed in sect. 3.2. In Fig. 7(b), the excessive electric field at the vicinity of the trench corners in device C1 can be efficiently moderated by the p-SRs in devices C5 and A2. Please note that similar peak values of the electric field can be observed in devices C5 and A2, indicating the p-SRs in both devices play a similar role in modulating the electric field around the trench corners. Therefore, embedding the p-SR at the corners of the trench is crucial for regulating the electric field and enhancing the blocking capability of the devices.

3.4. Transfer and on-state characteristics of the SR-MOSFETs

Figure 8(a) shows the transfer characteristics of the T-MOSFETs and SR-MOSFETs at a V_{DS} of 0.5 V, in which the SR-MOSFETs feature the same threshold voltage (V_{TH}) of 3.5 V as the T-MOSFETs, due to the identical p-doping concentration in the p-body and gate dielectric thickness (100 nm) for both devices.[27] The I_{DS} of the SR-MOSFETs is slightly smaller than that of the T-MOSFETs due to the narrower current conducting path with embedded JFET region at the vicinity of the trench gate. Figure 8(b) shows the output characteristics of the proposed SR-MOSFETs and the T-MOSFETs with V_{DS} swept from 0 to 10 V. The specific on-resistance ($R_{on,sp}$) of the proposed SR-MOSFETs (2.5 mΩ·cm^2) is slightly larger than that of the conventional T-MOSFETs (2.1 mΩ·cm^2), which agrees with the smaller I_{DS} of the SR-MOSFETs in Fig. 8(a). Please note that the I_{DS} first linearly increases and then saturates with increased V_{DS} in the conventional T-MOSFETs. The same phenomenon also exists in the SR-MOSFETs at low V_{GS}. Nevertheless, quasi-saturation (QS) effect occurs in the SR-MOSFETs at a high V_{GS} of 20 V, in which the I_{DS} keeps increasing with V_{DS} without saturation.

To investigate the mechanism of the QS effects above, we extract and compare the 2D electron distribution in the SR-MOSFETs with increased V_{DS} at different gate bias voltages, as shown in Figs. 9(a)–9(f). At a relatively small gate bias of 8 V in Figs. 9(a)–9(c), the depletion regions beneath the p-body layer and around the p-SRs gradually grow and merge with increased V_{DS}, leading to a pinched-off current path at the JFET region and thus saturated I_{DS} in the output curves. With a relatively larger gate bias of 20 V in Figs. 9(d)–9(f), more electrons are concentrated at the sidewall of the gate trench, suppressing the depletion extension from both the p-body and p-SR regions. Therefore, the current path at the JFET region remains open, causing QS effect in the SR-MOSFETs.

Moreover, the QS effect can also be investigated by analyzing the on-state current density in the JFET region ($J_{JFET} = n_e q v_e$), which determines the output current (I_{DS}) of the MOSFETs. As shown in Fig. 10, the electron concentration (n_e) and velocity (v_e) at the pinch-off point are determined for gate voltages of 8 V and 20 V, respectively. With a relatively large gate bias of 20 V in Fig. 10(a), the n_e first decreases with increased V_{DS} and then keeps rising before saturation. Meanwhile, v_e increases monotonously up to the electron saturation velocity of GaN in the drift region.[28] Therefore, the QS effects can be observed in the SR-MOSFETs at a relatively large gate bias of 20 V. On the other hand, the n_e gradually decreases with an increased V_{DS} at a relatively small gate bias of 8 V while v_e increases with V_{DS}, as shown in Fig. 10(b). Therefore, the corresponding I_{DS} saturates with the V_{DS} in the SR-MOSFETs at a relatively small gate bias of 8 V.

To precisely calculate the specific on-resistances ($R_{on,sp}$) of the conventional T-MOSFETs and proposed SR-MOSFETs, equivalent on-resistance models are re-derived based on B. J. Baliga's model,[29] as shown in Fig. 11. For high-voltage T-MOSFETs, the specific cathode contact resistance ($R_{C,sp}$), the specific source region resistance ($R_{S,sp}$) and the specific substrate resistance ($R_{SUB,sp}$) can be neglected.

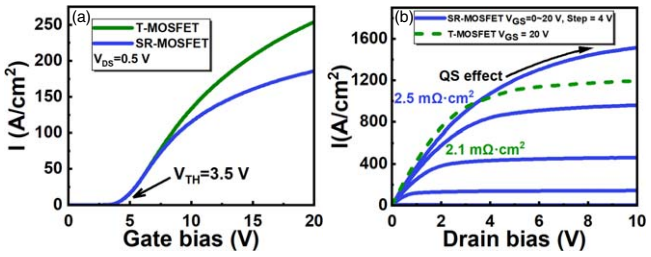

Fig. 8. (a) Transfer characteristics of the T-MOSFETs and SR-MOSFETs at a V_{DS} of 0.5 V. (b) Output characteristics of the T-MOSFETs and SR-MOSFETs.

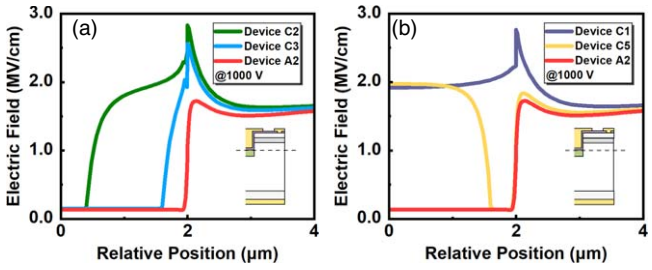

Fig. 7. (a) The lateral electric field profiles along the trench/p-SR interface of the devices at a V_{DS} of 1000 V in group A. (b) The lateral electric field profiles along the trench/p-SR interface of the devices at a V_{DS} of 1000 V in group B.

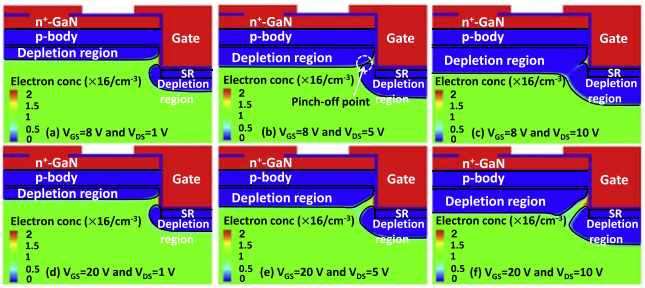

Fig. 9. Electron distribution in the SR-MOSFETs (a) at V_{GS} = 8 V and V_{DS} = 1 V, (b) at V_{GS} = 8 V and V_{DS} = 5 V, (c) at V_{GS} = 8 V and V_{DS} = 10 V, (d) at V_{GS} = 20 V and V_{DS} = 1 V, (e) at V_{GS} = 20 V and V_{DS} = 5 V, (f) at V_{GS} = 20 V and V_{DS} = 10 V.

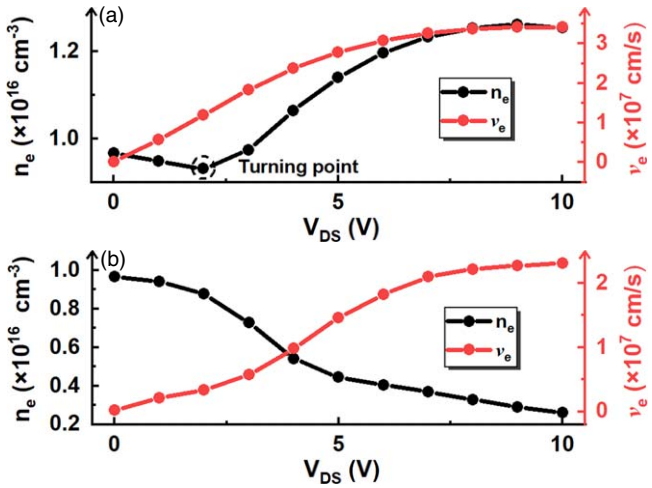

Fig. 10. (a) n_e and v_e at the pinch-off point for the SR-MOSFETs at a V_{GS} of 20 V. (b) n_e and v_e at the pinch-off point for the SR-MOSFETs at a V_{GS} of 8 V.

Therefore, the $R_{on,sp}$ for the T-MOSFETs is determined by the specific channel resistance ($R_{CH,sp}$) and the specific resistance of the drift region ($R_{DR,sp}$)[29]

$$R_{on,\mathrm{sp}} = R_{CH,\mathrm{sp}} + R_{DR,\mathrm{sp}}. \tag{3}$$

The $R_{CH,sp}$ is given by

$$R_{CH,sp} = \frac{L_{CH} \cdot P}{\mu_{CH} C_{ox} (V_{GS} - V_{TH})}, \tag{4}$$

where L_{CH} is the length of the channel determined by the thickness of the p-body region, P is half pitch of the cell, μ_{CH} is the electron mobility in the channel, and C_{ox} is the specific capacitance of the gate oxide, which is represented as

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}, \tag{5}$$

where ε_{ox} and t_{ox} are the dielectric constant and thickness of the gate oxide, respectively.

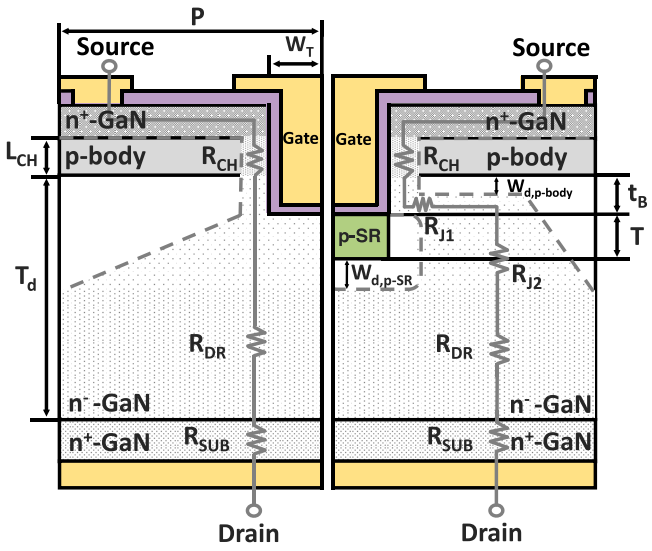

Fig. 11. Specific on-resistance model of T-MOSFETs (left) and SR-MOSFETs (right).

The $R_{DR,sp}$ is given by

$$R_{DR,sp} = \rho_{DR} P \ln\left(\frac{P}{W_T}\right) + \rho_{DR}(T_d - P + W_T) \tag{6}$$

where T_d is the thickness of the drift layer and W_T is the width of the gate trench, and the ρ_{DR} is expressed as

$$\rho_{DR} = \frac{1}{q\mu_{drift} N_d}. \tag{7}$$

The model for the low-field mobility[30] in the drift region is given by

$$\mu_{drift} = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + \left(\frac{N_d}{N_{ref}}\right)^{\beta}}, \tag{8}$$

where μ_{drift} is the electron mobility in the drift region, $\mu_{max} = 1460.7$ cm^2/(V·s), $\mu_{min} = 295$ cm^2/(V·s), $N_{ref} = 1 \times 10^{17}$ cm^{-3}, and $\beta = 0.66$.

The $R_{on,sp}$ for the proposed SR-MOSFETs is determined by $R_{CH,\mathrm{sp}}$, $R_{DR,\mathrm{sp}}$ and the specific JFET region resistance ($R_{JFET,sp}$). As shown in Fig. 11, $R_{JFET,sp}$ consists of two parts $R_{J1,sp}$ and $R_{J2,sp}$.

$$R_{on,\mathrm{sp}} = R_{CH,\mathrm{sp}} + R_{J1,\mathrm{sp}} + R_{J2,\mathrm{sp}} + R_{DR,\mathrm{sp}}. \tag{9}$$

The $R_{J1,sp}$ and $R_{J2,sp}$ are expressed as

$$R_{J1,sp} = \rho_{JFET} P \frac{W_{d,p-SR}}{t_B - W_{d,p-body}} \tag{10}$$

$$R_{J2,sp} = \rho_{JFET} P \frac{T + W_{d,p-\mathrm{SR}}}{P - W_T - W_{d,p-\mathrm{SR}}}, \tag{11}$$

where $W_{d,p-SR}$ is depletion width inner JFET region, $W_{d,p-body}$ is depletion width beneath the p-body region, and ρ_{JFET} is the resistivity of the JFET region, which is given by

$$\rho_{JFET} = \frac{1}{q\mu_{JFET} N_d} \tag{12}$$

Based on the on-state conduction models above, we calculated each component of the $R_{on,sp}$ for both T-MOSFETs and SR-MOSFETs with varying values of μ_{CH} ranging from 30 to 150 cm^2/(V·s) at a V_{DS} of 1 V and a V_{GS} of 20 V, as shown in Fig. 12. The SR-MOSFETs features a larger $R_{on,sp}$ due to the presence of the $R_{JFET,sp}$, as compared to the conventional T-MOSFETs. As μ_{CH} increases, the $R_{CH,sp}$ decreases rapidly in both T-MOSFETs and SR-MOSFETs while the $R_{DR,sp}$ remains almost unchanged. Specifically, with a μ_{CH} of 60 cm^2/V·s, the calculated $R_{on,sp}$ is 2.1 mΩ·cm^2 and 2.5 mΩ·cm^2 for the T-MOSFETs and SR-MOSFETs, respectively, which agrees well with the simulation results in Fig. 8(b). The good agreement indicates the effectiveness of the established models above.

4. Comparison between SR-MOSFET and conventional MOSFET with identical voltage levels for switching application

To evaluate the advantage of the proposed SR-MOSFETs for power applications, it is highly desirable to comprehensively compare the device performance of the SR-MOSFET and T-MOSFET with identical voltage levels. Therefore, we redesigned the structural parameters of the SR-MOSFET by

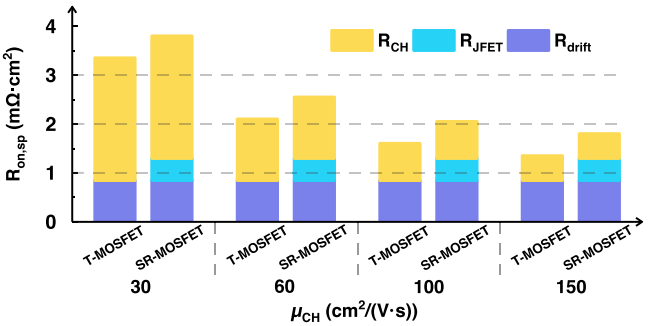

Fig. 12. Component and proportion of the specific on-resistance of the T-MOSFETs and the SR-MOSFETs with a varied μ_{CH} at a V_{DS} of 1 V and a V_{GS} of 20 V.

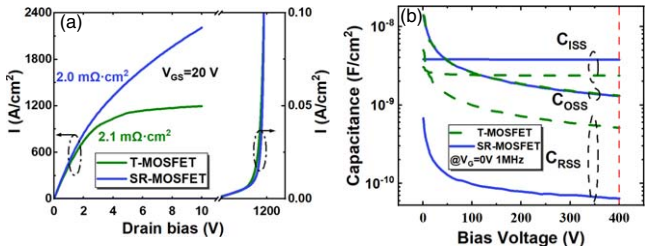

Fig. 13. (a) Output and breakdown characteristics of the T-MOSFET and SR-MOSFET. (b) The C_{ISS}, C_{OSS}, and C_{RSS} of the T-MOSFET and SR-MOSFET. The V_{GS} is fixed at 0 V.

decreasing the thickness of the drift layer from 12 μm to 7.4 μm and the thickness of the p-body layer from 0.55 μm to 0.4 μm, to get a comparable breakdown voltage as that of the T-MOSFET. The detailed parameters of the SR-MOSFET and T-MOSFET are shown in Table I. The p-SR structure of the vertical GaN power MOSFETs is grounded for efficient charge supply and extraction during switching.[23,24] Figure 13(a) compares the output characteristics of the T-MOSFET and SR-MOSFET. A slight decrease in the specific on-resistance can be observed from 2.1 mΩ·cm^2 in the T-MOSFET to 2.0 mΩ·cm^2 in the SR-MOSFET, which can result in a lower conduction loss during switching. Further reduction in the on-resistance of the SR-MOSFET can be anticipated by optimizing the thickness ratio of the p-GaN (R_{CH}) and the drift layer (R_{DR}), according to the on-resistance model established in Sect. 3.4. We also extracted the parasitic capacitances of the T-MOSFET and SR-MOSFET at a switching frequency of 1 MHz, as shown in Fig. 13(b). It can be observed that the output capacitance (C_{OSS}) remains unchanged. The input capacitance (C_{ISS}) of the SR-MOSFET is slightly higher than that of the T-MOSFET, while the reverse transfer capacitance (C_{RSS}) of SR-MOSFET is significantly reduced, compared with that from the T-MOSFET. To explain the phenomenon above, we plot schematics of parasitic capacitances and equivalent circuits from the T-MOSFET and SR-MOSFET. In Fig. 14, an additional C_{GD2} in series is introduced in the SR-MOSFET, which contributes to reduced C_{GD}(C_{RSS}). The increased C_{GS}(C_{ISS}-C_{RSS}) and C_{DS}(C_{OSS}-C_{RSS}) in SR-MOSFET are attributed to the introduction of parallel C_{GS2} and C_{DS2} by the p-SR, respectively.

C_{RSS} and C_{OSS} are critical parameters affecting the switching loss and switching speed. Figures 15(a) and 15(b) display the switching waves and switching energy loss of the T-MOSFET and SR-MOSFET at a supply voltage of 400 V and a current density of 100 A cm^{-2}, respectively. The double-pulse test (DPT) circuit is illustrated in the inset of Fig. 15(b). In the DPT circuit, the gate resistance (R_G) is set to be 10 Ω and V_{GS} toggles between −5 and 20 V to turn the device off and on, respectively. An ideal Schottky barrier diode, characterized by a capacitance (C) of 0 F, a breakdown voltage of 1200 V, a resistance (R) of 1×10^{-18} Ω and a transit time of 1 μs, is used to provide a freewheeling path. The load and stray inductances are 200 μH and 10 μH, respectively. We define the turn-on fall time (T_{on}) as the time taken for V_{DS} to fall from 90% to 10%, while the turn-off rise time (T_{off}) is defined as the time taken for V_{DS} to rise from 10% to 90%. It can be observed the T_{on} and T_{off} of the SR-MOSFET (21.6 and 19.4 ns) is significantly decreased than that of the T-MOSFET (30.8 and 23.3 ns), thanks to the smaller C_{RSS} in the SR-MOSFET. The turn-on energy loss (E_{on}) and turn-off energy loss (E_{off}) of the T-MOSFET and SR-MOSFET are calculated using Eqs. (13)-(15) below:[31]

$$E_{OSS} = \int_0^{V_{DD}} V_{DS} \times C_{OSS} dV_{DS} \tag{13}$$

$$E_{on} = \int_T^{T+T_{on}} I_{DS} \times V_{DS} dT + E_{oss} \tag{14}$$

$$E_{off} = \int_T^{T+T_{off}} I_{DS} \times V_{DS} dT - E_{oss} \tag{15}$$

Table I. Key device parameters for T-MOSFET and SR-MOSFET.

Symbol	Parameters	T-MOSFET	SR-MOSFET
T_{ox}	Thickness of oxide	100 nm	100 nm
$N_{p\text{-}body}$	Doping concentration of the p-body layer	2×10^{18} cm^{-3}	2×10^{18} cm^{-3}
T_{drift}	Thickness of the drift layer	12 μm	7.4 μm
N_{drift}	Doping concentration of drift layer	1×10^{16} cm^{-3}	1×10^{16} cm^{-3}
$T_{p\text{-}SR}$	Thickness of p-SR	—	0.2 μm
$N_{p\text{-}SR}$	Doping concentration of p-SR	—	9×10^{17} cm^{-3}
L_{ch}	Length of channel	0.55 μm	0.4 μm

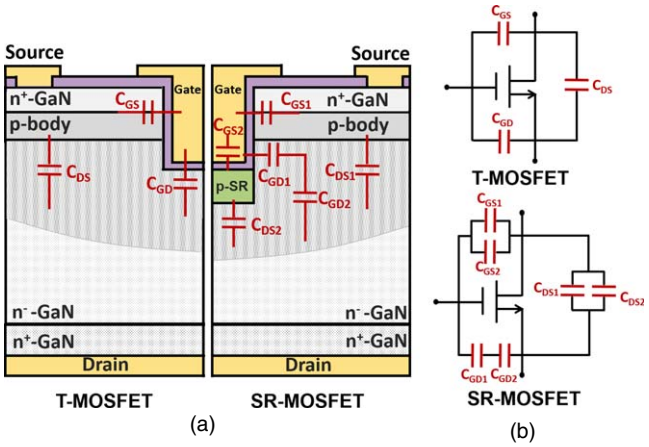

Fig. 14. (a) Schematics of parasitic capacitances of the T-MOSFET and SR-MOSFET. (b) Equivalent circuits of the T-MOSFET and SR-MOSFET.

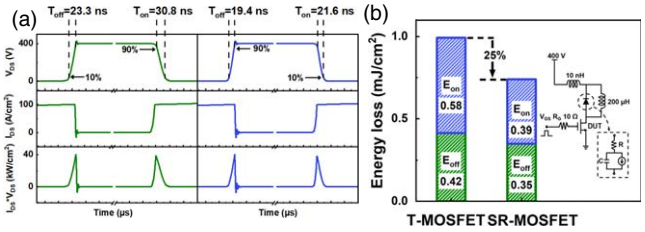

Fig. 15. (a) Switching waves of the T-MOSFET (left) and SR-MOSFET (right). (b) Switching energy loss of the T-MOSFET and SR-MOSFET. The inset shows the test circuit.

Both the E_{on} and E_{off} from the SR-MOSFET exhibit a significant decline compared with those from the T-MOSFET, resulting in a 25% reduction in total switching loss for the SR-MOSFET.

5. Conclusion

In summary, we systematically investigated the effects of the p-doping concentration, thickness, and width of the p-GaN shielding rings on the on-state and off-state characteristics of GaN power SR-MOSFETs. The RT and NRT behaviors in SR-MOSFETs are elucidated and a design strategy of the p-SRs is presented to achieve high gate stack reliability under NRT conditions. Moreover, we analyzed the QS effect for the output characteristics and established an on-state resistance model for the SR-MOSFETs. Superior dynamic performance is also observed for the SR-MOSFETs with identical voltage-level as conventional MOSFETs. The results are promising to provide theoretical guidance for the fabrication of high performance vertical GaN power MOSFETs towards high-voltage, high-power and HF power applications.

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